REMARKS

The following is intended as a full and complete response to the Office Action mailed on February 14, 2005. Claims 1-25 were examined. The Examiner rejected claims 1, 3-5, 14, 16 and 21 under 35 U.S.C. §102(b) as anticipated by Chu (U.S. Patent No. 5,530,798), claims 6, 10-13, 17, 19-20 and 23 under 35 U.S.C. §103(a) as obvious in view of Chu, claims 2, 15 and 22 under 35 U.S.C. §103(a) as obvious in view of Chu in combination with Morein (U.S. Patent No. 6,473,086) or Langendorf (U.S. Patent No. 6,760,031) and claim 25 under 35 U.S.C. §103(a) as obvious in view of Chu in combination with Rostoker (U.S. Patent No. 5,761,516). The Examiner also rejected claims 3 an 4 under 35 U.S.C. §112, second paragraph and further indicated that claims 7-9, 18 and 24 recite allowable subject matter.

Rejections under §112, Second Paragraph

The Examiner rejected claims 3 and 4 for having a confusing construction. In response, Applicants are amending the claims to more clearly delineate the relationship between the graphics processing module and the graphics processing unit. In view of these amendments, Applicant respectfully requests the withdrawal of the 35 U.S.C. §112, second paragraph rejection of the claims.

Rejections under 35 U.S.C. §102(b) and 35 U.S.C. §103(a)

Claim 1 recites the limitations of a clock generator that generates a clock signal and a controller configured to receive the clock signal, to compare the clock signal to a synchronization signal to generate a timing signal and to transmit the timing signal to a second graphics processing module. Chu does not teach or suggest these limitations.

Chu discloses a system of graphics processors, where a main graphics processor and at least one secondary graphics processor are arranged in cascaded fashion. Specifically, the disclosed system uses two heterogeneous sync signals to synchronize the cascaded graphics processors – a pixel sync signal (18) for synchronizing output color codes and layer codes and a picture field sync signal (19) for synchronizing a scan clock. See Chu at col. 2, lines 17-21. Each graphics processor includes a clock generator (40) for generating these two sync signals. The clock generator (40) includes a primary/secondary system synchronizer (60) to control the

signals output by the clock generator (40). See generally Chu at col. 2, lines 32-67. The Examiner argues that the primary/secondary system synchronizer (60) meets all of the limitations of the claimed controller. Applicants respectfully disagree with the Examiner's interpretation of Chu.

Figure 3 of Chu sets forth the structure of the primary/secondary system synchronizer (60), which includes a pixel sync signal I/O controller (57) and a picture field sync signal I/O controller (56). Each of these controllers may be configured as a tri-state I/O buffer. Specifically, the pixel sync signal I/O controller (57) is configured to output a dot_clock signal (102) generated by the clock generator (50) as the pixel sync signal (18), if a primary/secondary system select signal SD (122) indicates that the graphics processor that contains the clock generator (40) is the primary graphics processor in the system. However, the pixel sync signal I/O controller (57) is configured to input a pixel sync signal (18) received from the primary graphics processor in the system if the primary/secondary system select signal SD (122) indicates that the graphics processor that includes the clock generator (40) is the secondary graphics processor in the system. See Chu at col. 3, lines 1-12. Similarly, the picture field sync signal I/O controller (56) is configured to output a vertical blanking signal V_blank (120) generated by the vertical decoder (54) as the picture field sync signal (19), if the primary/secondary system select signal SD (122) indicates that the graphics processor that contains the clock generator (40) is the primary graphics processor in the system. However, the picture field sync signal I/O controller (56) is configured to input a picture field sync signal (19) received from the primary graphics processor in the system if the primary/secondary system select signal SD (122) indicates that the graphics processor that includes the clock generator (40) is the secondary graphics processor in the system. See Chu at col. 3, lines 12-19.

In the Office Action, the Examiner suggests that the primary/secondary system synchronizer (60) receives the dot_clock signal (102) (which the Examiner states is analogous to the claimed clock signal) and compares this signal to the vertical blanking signal V_blank (120) (which the Examiner states is analogous to the claimed synchronization signal) to generate and transmit a pixel sync signal (18) or a field sync signal (19) (which the Examiner states is analogous to the claimed timing signal). As the above description of the clock generator (40) clearly shows, though, the pixel sync signal I/O controller (57) and the picture field sync signal I/O controller (56) are two separately operating elements within the clock generator (40). They

each are configured to produce separate and distinct sync signals to the extent the graphics processor that includes the clock generator (40) is the primary graphics processor in the system. Thus, the description of Figure 3 makes clear that there is no comparison between the dot_clock signal (102) and the vertical blanking signal V_blank (120) in the primary/secondary system synchronizer (60), as suggested by the Examiner. In addition, none of the signals transmitted to (i.e., the signals input to) either the pixel sync signal I/O controller (57) or the picture field sync signal I/O controller (56) constitutes a synchronization signal. Therefore, there cannot be comparison of a clock signal and a synchronization signal in the primary/secondary system synchronizer (60), as recited in claim 1.

As the foregoing illustrates, Chu fails to teach or suggest the limitations of a controller that receives a clock signal, compares the clock signal to a synchronization signal, generates a timing signal and then transmits that timing signal to a second graphics processing module, recited in claim 1. Chu therefore cannot anticipate or render obvious claim 1. Further, neither Morein, Langendorf nor Rostoker cures the deficiencies of Chu described above. Thus, no combination of the cited references can render claim 1 obvious. For these reasons, Applicants respectfully submit that claim 1 and claims 2-13, dependent thereon, are in condition for allowance and request that the §102(b) and §103(a) rejections of these claims be withdrawn.

Independent claims 14 and 21 recite limitations similar to those discussed above in connection with allowable claim 1 and therefore are in condition for allowance for at least the same reasons as claim 1. Further, since claims 15-20 and claims 22-25 depend from allowable claims 14 and 21, respectively, these claims also are in condition for allowance.

Conclusion

Based on the above remarks, Applicants believe that they have overcome all of the objections and rejections set forth in the Office Action mailed on February 14, 2005 and that the pending claims are in condition for allowance. If the Examiner has any questions, please contact the Applicant's undersigned representative at the number provided below.

Respectfully submitted,

John C. Carey
Registration No. 51,530
MOSER, PATTERSON & SHERIDAN, L.L.P.
3040 Post Oak Blvd. Suite 1500
Houston, TX 77056
Telephone: (650) 330-2310
Facsimile: (650) 330-2314
Attorney for Applicants